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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/066,028	01/31/2002	Peter T. Liu	37310-000137	2099

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 12/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/066,028	LIU, PETER T.	
	Examiner	Art Unit	
	Quan Tra	2816	AW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17* is/are allowed.

6)☒ Claim(s) *1-5,7-16 and 18-20* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/13/2003 has been entered. A new ground of rejection is introduced.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 8-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8 is misdescriptive and renders the claim indefinite. It is misdescriptive for reciting "a validation circuit dynamically adjusting a validation point based one sense amplifier operating conditions...". It is not clear how the validation circuit "dynamically adjusting a validation point base on sense amplifier operating conditions" since the output of the sense amplifier is not coupled to the validation circuit. Figure 1 shows the validation circuit (70) has no relationship with the sense amplifier (50). The INVALID signal is for indicating the state of the power down signal (PDN). For example, when signal PDN is low, the INVALID signal is high, and when the PDN signal is low, the INVALID signal is high.

Claims 8-13 are rejected as including the indefiniteness of claim 8.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-5, 7-11, 14-16 and 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Aoki (USP 6125069).

As to claims 1, 8, and 14, Aoki discloses in figure 2 a buried fuse reading device, comprising: at least one buried fuse (10), at least one sense amplifier (17, 28, 32) sensing a condition of the buried fuse; and a validation circuit (the inverter in 38) indicating when the sense amplifier output is valid (when output of the inverter in 38 is low, the sense amplifier output is valid). As further called in for claim 14, the inverter in 38 tracks operation of the sense amplifier such that the inverter indicated when the sense amplifier has sufficiently settled on sense condition of the buried fuse (when output of the inverter is low, it indicate the sense circuits is enabled).

As to claim 2, figure 2 shows the validation circuit detects when the sense amplifier has sufficiently settled on a sensed condition of the buried fuse.

As to claim 3, 9 and 15, a circuit, not shown, that generating signal IN for powering the buried fuse reading device up and down; and wherein the validation circuit detects when the sense amplifier has sufficiently settled on a sensed condition once the power control circuit begins powering up the buried fuse reading device.

As to claims 4, 10, it is inherent for the circuit of figure 2 to have a bias generating circuit for generating first (Vdd) and second voltages (Vss); and wherein the sense amplifier operates based on the first and second voltages.

As to claims 5, 11, figure 2 shows the validation circuit operates based on the first and second voltages.

As to claim 7 and 13, Aoki's figure 15 further shows plurality of buried fuses (10s); and a sense amplifier (28s, 32s, 24s) associated with each of the buried fuses.

As to claim 16, figure 2 shows the sense amplifier (17) and the tracking circuit (inverter in 38) draw substantially no current when the power control circuit has the buried fuse reading device power down. (when, IN is low, one of the pull up and pull down circuits, not shown, in the inverter 17 in the inverter in 38 and must be turned off. Therefore, there is a gap between power supply and ground. Thus, the inverter circuits draw no current).

As to claim 18, figure 15 shows a buried fuse reading device, comprising at least one buried fuse (the buried fuse in circuit 22 at the left), at least one sense amplifier (28, 32 in circuit 22 at the left) sensing a condition of the buried fuse; and a validation circuit (10, 28, 32, 17, 18 in 22 at the right) mimicking, with a delay (10, 17, 18), the sense amplifier regardless of the state of the at least one buried fuse, and indicating when the sense amplifier output is valid (when the output of the validation circuit in the right is valid, it is indicated that the output of the sense amplifier in the left is also valid regardless the state of the sense amplifier).

As to claim 19, figure 15 shows the validation circuit is the same (they are both CMOS circuit) as the at least one sense amplifier but for the delay in the validation circuit.

As to claim 20, figure 15 shows the validation circuit is connected in parallel with the at least one sense amplifier and the at least one buried fuse.

Allowable Subject Matter

6. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claim 17 is allowed.

8. Claim 12 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

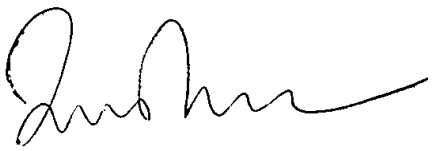
Claims 6 and 12 would be and claim 17 are allowable because the prior art fails to teach or suggest a circuit (such as figure 1) having a sense amplifier 50 includes first PMOS transistor (54) and a first NMOS transistor (56) connected in series with the buried metal fuse (52), a gate of the first PMOS transistor receiving the first voltage (BHI) and the gate of the first NMOS transistor receiving the second voltage (BLO); the validation circuit (70) includes a second PMOS transistor (72) and a second NMOS transistor (74) connected in series, a gate of the second PMOS transistor receiving the first voltage and a gate of the second NMOS transistor receiving the second voltage, the second PMOS and NMOS transistor being weaker than the first PMOS and NMOS transistors, respectively.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 703-308-6174. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



Quan Tra
Patent Examiner

December 15, 2003